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I am fluent in both the English and Japanese languages and capable of translating documents from one into the other of these languages.

The attached document is a true and accurate English translation to the best of my knowledge and belief of:

the specification of Japanese Patent Application No. 2001-338110 (2001)

I state that all statement made herein of my own knowledge are true and that all statements made on information and belief are believed to be true.

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[Title of the Invention] SEMICONDUCTOR DEVICE AND METHOD FOR MANUFACTURING THE SAME

[Scope of Claim for Patent]

[Claim 1]

A method for manufacturing a semiconductor device comprising:

an on-substrate connecting step of connecting face down a semiconductor chip having an active surface formed with a recess arranging a conductor therein onto one surface of a semiconductor substrate; and

a step of polishing or abrading an inactive surface of the semiconductor chip to expose the conductor in the inactive surface of the semiconductor chip after the on-substrate connecting step.

[Claim 2]

A method for manufacturing a semiconductor device according to claim 1,

wherein the semiconductor substrate is a semiconductor wafer, and

the on-substrate connecting step includes a step of arranging and connecting the semiconductor chips in plurality side by side on the semiconductor wafer,

the method further comprising a step of cutting the semiconductor wafer based on a predetermined region including

at least one of the semiconductor chips to obtain a semiconductor device having a chip-on-chip structure.

[Claim 3]

A method for manufacturing a semiconductor device according to claim 1 or 2, wherein the one surface of the semiconductor substrate is an active surface, further including a substrate polish step of polishing or abrading the inactive surface of the semiconductor substrate to reduce the thickness thereof.

[Claim 4]

A method for manufacturing a semiconductor device according to claim 3,

wherein the semiconductor substrate has an active surface formed with a recess arranging a conductor therein, and

the substrate polish step includes a step of polishing or abrading the inactive surface of the semiconductor substrate to expose the conductor of the semiconductor substrate in the inactive surface of the semiconductor substrate.

[Claim 5]

A method for manufacturing a semiconductor device according to any one of claims 1 to 4, further comprising an on-chip connecting step of connecting another semiconductor chip on the semiconductor chip.

[Claim 6]

A method for manufacturing a semiconductor device according to claim 5,

wherein the other semiconductor chip has an active surface formed with a recess arranging a conductor therein, and

the on-chip connecting step is to connect face down the other semiconductor chip on the semiconductor chip,

the method further comprising a step of polishing or abrading an inactive surface of the other semiconductor chip to expose the conductor of the other semiconductor chip in the inactive surface of the other semiconductor chip.

[Claim 7]

A method for manufacturing a semiconductor device comprising:

a step of connecting a semiconductor chip on an active surface of a semiconductor substrate having an active surface formed with a recess arranging a conductor therein; and

a step of polishing or abrading an inactive surface of the semiconductor substrate to expose the conductor of the semiconductor substrate in the inactive surface of the semiconductor substrate.

[Claim 8]

A method for manufacturing a semiconductor device comprising:

an on-substrate connecting step of connecting a semiconductor chip face down on a semiconductor substrate; and

a step of polishing or abrading an inactive surface of the semiconductor chip to reduce a thickness of the semiconductor chip after the on-substrate connecting step.

[Claim 9]

A semiconductor device having a structure superposed with a plurality of semiconductor chips,

wherein at least one of the semiconductor chips has a penetration hole arranging a conductor therein and penetrating the semiconductor chip in the thickness direction.

[Claim 10]

A semiconductor device according to claim 9, wherein the plurality of semiconductor chips include a first semiconductor chip having a first penetration hole arranging a conductor therein and a second semiconductor chip superposed adjacent to the first semiconductor chip and having a second penetration hole arranging a conductor therein in a position deviated from the first penetration hole.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to a semiconductor device

of a chip-on-chip structure that has a semiconductor chip bonded with another semiconductor chip thereon, and to a method for manufacturing the same.

[0002]

[Prior Art]

There are semiconductor devices increased in integration degree, including system-on-chips (SOCs) and multi-chip-modules (MCMs). In the system-on-chip, the functions conventionally realized on a plurality of ICs are integrated on one semiconductor chip. The multi-chip-module is structured by a plurality of semiconductor chips arranged with density on a wiring board of glass-epoxy or the like. Each of them has multiple functions as one semiconductor device and can be size-reduced as compared to a combination of a plurality of semiconductor devices realizing the equivalent functions. Meanwhile, this reduces the wiring length in the overall, enabling high-speed transmission of signals.

[0003]

[Problems to be solved by the Invention]

However, the system-on-chip is complicated in manufacture process, requiring a huge amount of capital investment and hence high manufacture cost. Meanwhile, the multi-chip-module has a plurality of semiconductor chips mutually arranged side by side on a wiring board. Because

these semiconductor chips are connected by wirings, the size is greater as compared to the system-on-chip and hence integration degree lowers.

[0004]

It is therefore an object of the present invention to provide a manufacturing method for obtaining a semiconductor device increased in integration degree.

It is another object of the invention to provide a manufacturing method for a semiconductor device low in manufacture cost.

It is still another object of the invention to provide a semiconductor device increased in integration degree.

[0005]

It is further another object of the invention to provide a semiconductor device low in manufacture cost.

[0006]

[Means to Solve the Problems and Effects of the Invention]

An invention according to claim 1 for solving the above problems is a method for manufacturing a semiconductor device comprising: an on-substrate connecting step of connecting face down a semiconductor chip (1, 15) having an active surface (2a, 3a) formed with a recess (22, 33) arranging a conductor therein onto one surface of a semiconductor substrate; and a step of polishing or abrading an inactive surface of the semiconductor chip to expose the conductor in

the inactive surface of the semiconductor chip after the on-substrate connecting step.

[0007]

The alpha-numerals in parentheses denote components in the embodiment to be described, consistently in this section.

In the semiconductor chip or substrate, the active surface is a surface forming functional elements or wiring thereon while the inactive surface is a surface on a side opposite to the active surface. To connect face down refers to connect a semiconductor chip or the like to a connection member (e.g. semiconductor substrate) with the active surface of the semiconductor chip or the like opposed to the connection member.

[0008]

The conductor member may be filled in the recess of the semiconductor chip (first semiconductor chip) or arranged in a part of the recess (e.g. along an inner peripheral wall) in a thickness direction of the first semiconductor chip. In the case the conductor is filled in the recess, the conductor can be formed by using a conductor paste. The conductor can be connected to a wiring provided on the active surface of the first semiconductor chip. An internal-connection electrode may be provided on the active surface of the first semiconductor chip.

[0009]

the inactive surface of the semiconductor chip after the on-substrate connecting step.

[0007]

Alpha-numerals in parentheses denote components in an embodiment to be described, consistently in this section.

In the semiconductor chip or substrate, the active surface is a surface forming functional elements or wiring thereon while the inactive surface is a surface on a side opposite to the active surface. To connect face down refers to connect a semiconductor chip or the like to a connection member (e.g. semiconductor substrate) with the active surface of the semiconductor chip or the like opposed to the connection member.

[0008]

The conductor member may be filled in the recess of the semiconductor chip (first semiconductor chip) or arranged in a part of the recess (e.g. along an inner peripheral wall) in a thickness direction of the first semiconductor chip. In the case the conductor is filled in the recess, the conductor can be formed by using a conductor paste. The conductor can be connected to a wiring provided on the active surface of the first semiconductor chip. An internal-connection electrode may be provided on the active surface of the first semiconductor chip.

[0009]

The semiconductor substrate may be a semiconductor chip (second semiconductor chip). Alternatively, the semiconductor substrate may be a substrate greater in size and including an area corresponding to the second semiconductor chip. Due to this, obtained is a semiconductor device having a chip-on-chip structure in which the first and second semiconductor chips are joined together.

By connecting face down the first semiconductor chip on one surface of the semiconductor substrate, the first semiconductor chip is placed in a state the active surface faces the semiconductor substrate while the inactive surface is open. Consequently, it is easy, in this state, to polish or abrade the inactive surface of the first semiconductor chip.

[0010]

By polishing or abrading the inactive surface of the first semiconductor chip to expose the conductor, obtained is a penetration hole penetrating the first semiconductor chip in the thickness direction. Owing to the conductor arranged in the penetration hole, the penetration hole serves as a via hole or through-hole to electrically connecting the active surface of the first semiconductor chip and the inactive surface thereof. Meanwhile, even after exposing the conductor, polish or abrasion may be continued to obtain a desired thickness of the first semiconductor chip. This

can reduce the thickness of the semiconductor device entirely. Polish may be by a physical process or may be a chemical polish such as etching.

[0011]

A step may be included of sealing the first semiconductor chip with an insulator after the on-substrate connecting step. The insulator may be a resin (e.g. polyimide), for example. The insulator may cover or expose the inactive surface of the first semiconductor chip to seal the first semiconductor chip. In the case sealing is done with the insulator covering the inactive surface of the first semiconductor chip, it is possible to carry out a step that, after the insulator existing on the inactive surface is removed by a step of polish, abrasion, cutting or etching, the inactive surface of the first semiconductor chip is polished or abraded simultaneously with the insulator to expose the conductor.

[0012]

The first semiconductor chip is mechanically protected by being sealed with the insulator. It is, accordingly, possible to prevent the first semiconductor chip from being broken or the connection between the first semiconductor chip and the semiconductor substrate from being damaged due to the stress caused upon polishing or abrading the first semiconductor chip thereafter. Thus, the first

semiconductor chip can be made small in thickness.

Through the conductor exposed in the inactive surface of the first semiconductor chip, connection is possible with a wiring or another semiconductor chip. Thereby, the active surface of the first semiconductor chip can be connected to another semiconductor chip at a short distance. Therefore, a semiconductor device obtained by such a manufacturing method can be made small in size with higher integration degree.

[0013]

The semiconductor device obtained by such a manufacturing method is structured with a combination of a plurality of semiconductor chips (first and second semiconductor chips, etc.), similarly to the multi-chip-module. Namely, manufacture cost is low because of difference from the integration of all the functions on one semiconductor chip as in the system-on-chip.

An invention according to claim 2 is a method for manufacturing a semiconductor device according to claim 1, wherein the semiconductor substrate is a semiconductor wafer (15), and the on-substrate connecting step includes a step of arranging and connecting the semiconductor chips in plurality in a sideway direction on the semiconductor wafer and a step of cutting the semiconductor wafer based on a predetermined region including at least one of the

semiconductor chips to obtain a semiconductor device having a chip-on-chip structure.

[0014]

The semiconductor wafer may be arranged with a multiplicity of regions (predetermined regions) each corresponding to the second semiconductor chip. By this manufacturing method, it is possible to carry out an on-substrate connecting step or conductor exposing step, in batch, on the region corresponding to a plurality of second semiconductor chip. By cutting a semiconductor wafer on which these steps have been done, it is possible to manufacture a plurality of semiconductor devices of a chip-on-chip structure with efficiency. That is, this manufacturing method makes it possible to obtain a semiconductor device low in manufacture cost.

[0015]

In a case where the on-substrate connecting step is to arrange and connect a plurality of first semiconductor chips side by side in a region of the semiconductor wafer corresponding to the second semiconductor chip (one semiconductor device), it is possible to obtain a semiconductor device having a structure in which a plurality of first semiconductor chips are arranged side by side on the second semiconductor chip. In this case, the recesses arranging a conductor therein may be formed in the active

surfaces of all the first semiconductor chips or may be formed only in the active surfaces in part of the first semiconductor chips.

[0016]

In a case where this manufacturing method includes a step of connecting one or a plurality of other semiconductor chips (third semiconductor chips or the like) on at least one first semiconductor chip, it is possible to obtain a semiconductor device forming a plurality of blocks each structured with one or a plurality of vertically superposed semiconductor chips on the semiconductor substrate. Such a semiconductor device is high in integration degree.

An invention according to claim 3 is a method for manufacturing a semiconductor device according to claim 1 or 2, wherein the one surface of the semiconductor substrate is an active surface (1a) and the method further including a substrate polish step of polishing or abrading the inactive surface of the semiconductor substrate to reduce the thickness thereof.

[0017]

The semiconductor substrate may have a sufficient thickness in order not to be readily broken during the steps. In this case, it is still possible to sufficiently reduce the thickness of the second semiconductor chip finally obtained by the substrate polish step. This can make the semiconductor

device small in size and enhance the integration degree thereof.

The substrate polish step can be carried out by a method similar to that of the first semiconductor chip.

[0018]

An invention according to claim 4 is a method for manufacturing a semiconductor device according to claim 3, wherein the semiconductor substrate is formed, in the active surface, with a recess (21) arranging a conductor (1d) therein, and the substrate polish step includes a step of polishing or abrading the inactive surface of the semiconductor substrate to expose the conductor within the semiconductor substrate at the inactive surface of the semiconductor substrate.

The conductor in the semiconductor substrate may be filled in the recess or arranged in a part of the recess in a thickness direction of the semiconductor substrate. The conductor can be connected to a wiring provided on the active surface of the semiconductor substrate formed with the recess.

[0019]

By polishing or abrading the inactive surface of the semiconductor substrate forming the recess in the active surface to expose the conductor, it is possible to obtain a penetration hole penetrating the semiconductor substrate in

the thickness direction. Because the conductor is arranged in the penetration hole, the penetration hole in a final form of semiconductor device can play a role as a via hole or through-hole electrically connecting the active surface and the inactive surface of the second semiconductor chip. After exposing the conductor, polish or abrasion may be continued until the semiconductor substrate becomes sufficiently small in thickness. This can reduce the thickness of the second semiconductor chip and hence of the entire semiconductor device, and further shorten the wiring length between the active surface and the inactive surface of the semiconductor substrate (conductor length).

[0020]

Prior to the step of polishing or abrading the semiconductor substrate, a step of sealing the first semiconductor chip with an insulator may be carried out. In this case, the semiconductor substrate is reinforced by the insulator or the first semiconductor chips. Accordingly, when the semiconductor device in such as state is polished or abraded, it is not readily broken. Therefore, the semiconductor substrate can be made small in thickness.

A step may be included of forming a bump (for example, connecting solder ball) as an external-connection electrode on the inactive surface of the semiconductor substrate (second semiconductor chip). Where the conductor is filled

within the penetration hole of the semiconductor substrate, the external-connection electrode may be directly connected to the conductor. Alternatively, a wiring may be formed on the inactive surface of the semiconductor substrate to connect the external-connection electrode and the conductor in the penetration hole via the wiring. The semiconductor device obtained can be directly connected on another wiring board or the like through the external-connection on another wiring board or the like through the external-connection electrodes. Namely, such a semiconductor device can be reduced in size because of the unnecessity of an interposer for externally connecting the semiconductor chip as required in the multi-chip-module.

[0021]

An invention according to claim 5 is a method for manufacturing a semiconductor device according to any one of claims 1 to 4 further comprising an on-chip connecting step of connecting another semiconductor chip (4 - 8) onto the semiconductor chip.

The other semiconductor chip (third semiconductor chip) may have an internal-connection electrode on the active surface. In this case, the internal-connection electrode of the third semiconductor chip may be directly connected to the conductor exposed in the inactive surface of the first semiconductor chip or be connected through a wiring or

electrode pad. The conductor in the first semiconductor chip can connect the inactive surface of the first semiconductor chip and the active surface of the third semiconductor chip at a short distance (in the shortest, nearly a thickness of the first semiconductor chip). The wiring length is shortened by reducing the thickness of the first semiconductor chip due to polish or abrasion.

[0022]

An invention according to claim 6 is a method for manufacturing a semiconductor device according to claim 5, wherein the other semiconductor chip has an active surface (4a, 5a, 7a, 8a) formed with a recess (24, 25, 27, 28) arranging a conductor therein, the on-chip connecting step is to connect face down the other semiconductor chip on the semiconductor chip, the method further including a step of polishing or abrading the inactive surface of the other semiconductor chip to expose the conductor of within the other semiconductor chip at the inactive surface of the other semiconductor chip.

[0023]

By connecting face down the other semiconductor chip (third semiconductor chip) on the semiconductor chip (first semiconductor chip), the third semiconductor chip is placed in a state that its active surface faces the first semiconductor chip while its inactive surface is open. Consequently, it is possible in this state to polish or abrade

the inactive surface of the third semiconductor chip.

By this manufacturing method obtained is a penetration hole penetrating the third semiconductor chip in the thickness direction. Still another semiconductor chip or wiring may be arranged on the third semiconductor chip. In this case, electrical connection can be made at a short wiring length between the active surface of the third semiconductor chip and the other semiconductor chip or wiring through the penetration hole of the third semiconductor chip as a via hole or through-hole.

[0024]

Because it is possible to arbitrary define a recess providing position on the inactive surface of the first and third semiconductor chips, the penetration holes in the first and third semiconductor chips are independent in position of each other in an obtained semiconductor device. Namely, in the obtained semiconductor device, the penetration hole of the third semiconductor chip can be in a position immediately above the penetration hole of the first semiconductor chip or in a position other than that.

The conductors of the first semiconductor chip and third semiconductor chip, in the obtained semiconductor device, may each directly connected to form a common electrode. Alternatively, such a common electrode may not be formed. In a case where each of the first and third semiconductor chips

has a plurality of recesses, the penetration holes in plurality respectively arranging conductors therein are obtained in each of the first and third semiconductor chips. In this case, the conductors of the first semiconductor chip and third semiconductor chip may form common electrodes, in part of combinations. Alternatively, all the combinations may form common electrodes. Alternatively, no common electrodes may be formed.

[0025]

After exposing the conductor, polish or abrasion may be continued to reduce the thickness until the third semiconductor chip has a desired thickness. This can reduce the thickness of the entire semiconductor device.

Similarly, a step may be carried out of connecting yet another semiconductor chip (fourth semiconductor chip) on the third semiconductor chip. A recess arranging a conductor therein may be formed in an active surface of the fourth semiconductor chip. In this case, a process may be carried out that, after connecting face down the fourth semiconductor chip onto the third semiconductor chip, an inactive surface of the fourth semiconductor chip is polished or abraded to expose the conductor in the fourth semiconductor chip in its inactive surface. By repeating such a process, it is possible to obtain a semiconductor device having a structure in which a plurality of semiconductor chips are vertically superposed

on the semiconductor substrate. The semiconductor chips adjacent in the superposing direction are electrically connected with each other at a short wiring length by the conductors in the penetration holes. Such a semiconductor substrate has a high integration degree.

[0026]

An invention according to claim 7 is a method for manufacturing a semiconductor device comprising: a step of connecting a semiconductor chip (2, 3) on an active surface of a semiconductor substrate (1, 15) formed, in the active surface (1a), with a recess (21) arranging a conductor (1d) therein; and a step of polishing or abrading an inactive surface of the semiconductor substrate to expose the conductor within the semiconductor substrate at the inactive surface of the semiconductor substrate.

This semiconductor device manufacturing method makes it possible to obtain a semiconductor device short in external-connection wiring length (conductor length) but high in integration degree. The semiconductor device obtained by such a manufacturing method is structured with a combination of a plurality of semiconductor chips, similarly to the multi-chip-module. Namely, manufacture cost is low because of difference from the integration of all the functions on one semiconductor chip as in the system-on-chip.

[0027]

An invention according to claim 8 is a method for manufacturing a semiconductor device comprising: an on-substrate connecting step of connecting face down a semiconductor chip (2, 3) on a semiconductor substrate (1, 15); and a step of polishing or abrading an inactive surface of the semiconductor chip to reduce a thickness of the semiconductor chip after the on-substrate connecting step.

By the on-substrate connecting step, the semiconductor chip is placed in a state that its active surface faces the semiconductor substrate while the inactive surface is open. Accordingly, it is possible in this state to easily polish or abrade the inactive surface of the semiconductor chip.

[0028]

Because this manufacturing method can reduce the thickness of the semiconductor chip, it is possible to obtain a semiconductor device small in thickness but high in integration degree.

An invention according to claim 9 is a semiconductor device having a structure with a plurality of semiconductor chips (1 - 8) superposed, wherein at least one of the semiconductor chips has a penetration hole (1c - 5c, 7c, 8c) arranging a conductor (1d - 5d, 7d, 8d) therein and penetrating the semiconductor chip in a thickness direction.

[0029]

A method for manufacturing a semiconductor device according to any one of claims 1 to 8 makes it possible to obtain such a semiconductor device. Such a semiconductor device is high in integration degree but low in manufacture cost.

An invention according to claim 10 is a semiconductor device according to claim 9, wherein the plurality of semiconductor chips include a first semiconductor chip having a first penetration hole arranging a conductor therein and a second semiconductor chip superposed adjacent to the first semiconductor chip and having a second penetration hole arranging a conductor therein in a position deviated from the first penetration hole.

[0030]

A method for manufacturing a semiconductor device according to claim 6 makes it possible to obtain such a semiconductor device.

The second semiconductor chip may have a plurality of second penetration holes. In this case, every second penetration hole may be arranged in a position deviated from the first penetration hole. In this case, the conductor arranged in the first penetration hole is in a position deviated from the conductor arranged in the second penetration hole. Accordingly, it is easy to provide a structure such that the conductor in the first semiconductor

chip is not in direct connection (not to form a common electrode) with the conductor in the second semiconductor chip. Such a semiconductor device has a high degree of design freedom.

[0031]

[Embodiment of the Invention]

An embodiment of the present invention is explained in detail below with reference to the accompanying drawings.

Fig. 1 is a schematic sectional view showing a structure of a semiconductor device according to an embodiment of the present invention.

Chip blocks 11, 12 each having a plurality of semiconductor chips (child chips) vertically superposed one upon another are connected on a parent chip 1, which is one semiconductor chip. The chip block 11 includes four child chips 2, 4, 5, 6 arranged one over another from a proximate end toward a distal end to the parent chip 1. The chip block 12 includes three child chips 3, 7, 8 arranged one over another from a proximate end toward a distal end to the parent chip 1. On the parent chip 1, polyimide resin 10 covers laterally the chip blocks 11, 12 and over the chip block 12. This constitutes the semiconductor device substantially in a cuboid.

[0032]

The parent chip 1, the child chip 2 and the child chip

3 have opposed surfaces respectively made as active surfaces 1a, 2a and 3a. Herein, the active surface is a surface forming functional elements and wirings thereon. The child chips 4 - 8 respectively have active surfaces 4a - 8a at their lower surfaces (surfaces close to the parent chip 1). The semiconductor chip (parent chip 1 or child chip 2 - 8) has an inactive surface opposite to the active surface, having no functional elements formed thereon. Namely, the child chips 2 - 8 are connected face down on the parent chip 1 or child chip 2 - 5, 7. The active surface 1a - 8a has an internal-connection electrode 1b - 8b.

[0033]

The child chip 2 - 5, 7, 8 has a penetration hole (via hole) 2c - 5c, 7c, 8c penetrating through it in a thickness direction. The penetration hole 2c - 5c, 7c 8c is filled therein with an electrical conductor 2d - 5d, 7d, 8d. The conductor 2d - 5d, 7d, 8d is electrically connected to a wiring (not shown) formed on the active surface 2a - 5a, 7a, 8a of the child chip 2 - 5, 7, 8. The child chip 6, positioned in the uppermost of the chip block 11, is not provided with a penetration hole.

[0034]

The conductor 2d - 5d, 7d, at its top end, is connected with an electrode pad 2e -5d, 7e. Also, some of the conductors 2d, 3d, 5d, 7d, at their top ends, are connected with any of

intralevel wirings Lh1, Lh2, Lh31 in place of the electrode pad. The conductor 8d, at its top end, is connected with an intralevel wiring Lh32.

The internal-connection electrode 2b, 3b of the child chip 2, 3 is connected to the internal-connection electrode 1b of the parent chip 1. The internal-connection electrode 4b of the child chip 4 is connected to either of the electrode pad 3e or the intralevel wiring Lh1 provided on the upper surface (inactive surface) of the child chip 3. Similarly, the internal-connection electrode 5b - 8b is connected to either of the electrode pad 4e, 5e, 3e, 7e or the intralevel wiring Lh1, Lh2, Lh31 provided on the upper surface of the adjacent child chip 4, 5, 3, 7.

[0035]

The child chip 2 at its upper surface (inactive surface) and the child chip 3 at its upper surface are nearly on the common plane (on the first wiring plane 31). The intralevel wiring Lh1 is provided in a manner extending on the plane. The child chip 4 at its upper surface and the child chip 7 at its upper surface are nearly on the common plane (on the second wiring plane 32). The intralevel wiring Lh2 is provided in a manner extending on this plane. The child chip 5 at its upper surface and the child chip 8 at its upper surface are nearly on the common plane (on the third wiring plane 33). The intralevel wirings Lh31, Lh32 are provided in a manner

extending on this plane. Also, an interlevel wiring Lv having a funnel form (V-form in section) is formed extending between the planes respectively including the second wiring plane 32 and the third wiring plane 33.

[0036]

The intralevel wiring Lh1 is connected to the conductor 2d and internal-connection electrodes 4b, 7b. Namely, the child chips 2, 4, 7 are mutually electrically connected by the intralevel wiring Lh1. The intralevel wiring Lh2 is connected to the conductor 7d, the internal-connection electrode 8b and the interlevel wiring Lv. The interlevel wiring Lv is integrally formed with the intralevel wiring Lh31, and the intralevel wiring Lh31 is connected to the internal-connection electrode 6b. Namely, the child chips 6 - 8 are mutually electrically connected by the intralevel wiring Lh2, Lh31 and interlevel wiring Lv. The intralevel wiring Lh 32, at its point outside the section shown Fig. 1, is connected to other child chips via the other intralevel wirings (and interlevel wirings).

[0037]

The parent chip 1 is formed with a penetration hole 1c penetrating the parent chip 1 in a thickness direction. The penetration hole 1c is filled therein with a conductor 1d. The conductor 1d is connected to a wiring (not shown) formed on the active surface 1a. The conductor 1d, at its bottom

end (close to the inactive surface of the parent chip 1), is connected to a bump 9 nearly in a spherical form. Namely, the wiring formed on the active surface 1a and the bump 9 are electrically connected together by the conductor 1d. Through the bumps 9, the semiconductor device can be directly mounted on a wiring board. Namely, the semiconductor device like this can be reduced in size because of not requiring an interposer for externally connecting a semiconductor chip, such as a multi-chip-module (MCM) wiring board.

[0038]

This semiconductor device is structured with a combination of a plurality of semiconductor chips (parent chip 1 and child chips 2 - 8), just like a multi-chip-module. Namely, this does not integrate all the functions on one semiconductor chip as in the system-on-chip (SOC), and hence is low in manufacture cost.

In the semiconductor device thus structured, the child chip 2 - 5, 7 is in electrical connection with the other child chips 2 - 8 adjacent to the above and below, through the conductors 2d - 5d, 7d filled in the penetration holes 2c - 5c, 7c. Accordingly, the wiring length between the child chips 2 - 8 mutually adjacent in the superposing direction is minimally nearly equal to the thickness of the child chip 2 - 5, 7, hence being short in wiring distance.

[0039]

Furthermore, direct connection is provided between the child chips 2, 4 - 6 constituting the chip block 11 and the child chips 3, 7, 8 constituting the chip block 12 by the intralevel wirings Lh1, Lh2, Lh31, Lh32 and interlevel wiring Lv, thus giving a short wiring length between them. This is because, in the case of an absence of the intralevel wirings Lh1, Lh2, Lh31, Lh32 and interlevel wiring Lv, connection must be made between the child chips 2, 4 - 6 constituting the chip block 11 and the child chip 3, 7, 8 constituting the chip block 12 necessarily through the wiring formed on the active surface 1a of the parent chip 1.

[0040]

For example, considered is a case to connect between the child chip 6 and the child chip 7. First, in order to connect the child chip 6 to the wiring formed on the active surface 1a, connection must be via the electrode pad 5e, the conductor 5d, the wiring formed on the active surface 5a, the internal-connection electrode 5b, the electrode pad 4e, the conductor 4d, the wiring formed on the active surface 4a, the internal-connection electrode 4b, the electrode pad 2e, the conductor 2d, the internal-connection electrode 2b and the internal-connection electrode 1b. Furthermore, in order to connect the wiring formed on the active surface 1a and the child chip 7, connection must be via the internal-connection electrode 1b, the internal-connection electrode 3b, the

wiring formed on the active surface 3a, the conductor 3d and the electrode pad 3e. Thus, there encounters an increase in wiring length in both directions vertical to and parallel with the active surface 1a.

[0041]

On the contrary, in the present semiconductor device, the child chip 6 and the child chip 7 are connected together through only the internal-connection electrode 6b, intralevel wiring Lh 31, interlevel wiring Lv and intralevel wiring Lh2. Accordingly, the wiring length is short in both directions vertical to and parallel with the active surface 1a.

The electrical connection between the child chip 2 and the child chip 3 can also be reduced in wiring length by the wiring formed on the active surface 1a of the parent chip 1. However, by providing a connection between the child chip 2 and the child chip 3 at least in part thereof through the intralevel wiring Lh, wiring can be dispersed with a result of wiring with density. Similarly, although the child chip 8 and the other child chip 2 - 7 can be connected through the intralevel wiring Lh2 arranged on the active surface 8a of the child chip 8, a wiring made from the inactive surface of the child chip 8 via the conductor 8d can disperse with a result of wiring with density.

[0042]

Meanwhile, the parent chip 1 is short in the wiring length for external connection because external connection is via the conductor 1d filled in the penetration hole 1c and the bump 9. The conductor 1d can be decreased in the length in thickness direction of the parent chip 1 by making the parent chip 1 small in thickness.

As described above, the semiconductor device can transmit signals at high speed because of its short wiring length. Also, the semiconductor device is high in integration degree because its thickness can be configured small. Meanwhile, because arbitrary two of the child chips 2 - 8 can be connected at a short wiring length by the intralevel wirings Lh1, Lh2, Lh31, Lh32 and interlevel wiring Lv, there is more design freedom of semiconductor device.

[0043]

The conductor 1d - 5d, 7d, 8d may be provided in part of the internal space of the penetration hole 1c - 5c, 7c, 8c (e.g. along the inner peripheral wall). It is possible to desirably determine a position of the penetration holes 1c - 5c, 7c, 8c in the parent chip 1 and child chips 2 - 5, 7, 8. Namely, the penetration hole 2c - 5c, 7c, 8c of the child chip 2 - 5, 7, 8 is arranged regardless of (or in different position from) the position of the adjacent below one of the penetration hole 1c of the parent chip 1 and the penetration hole 2c, 4c, 3c, 7c of the child chip 2, 4, 3,

7. Of course, these may be arranged in a relationship of immediately above/below.

[0044]

The conductor 2d - 5d, 7d, 8d of the child chip 2 - 5, 7, 8 may be directly connected to form a common electrode with the adjacent below one of the conductor 1d of the parent chip 1 or with the conductor 2d, 4d, 3d, 7d of child chip 2, 4, 3, 7. Alternatively, they may not form such a common electrode. Meanwhile, of these conductors 1d - 5d, 7d, 8d, some combinations may form common electrodes or all the combinations may form common electrodes. Alternatively, no common electrodes may be formed.

[0045]

It is possible to define the number of child chips 2 - 8 structuring the chip block 11, 12, i.e. the number may be one or a plurality. The intralevel wirings Lh1, Lh2, Lh31, Lh32 and the interlevel wiring Lv can be provided to connect arbitrary one of the child chips 2, 4 - 6 constituting the chip block 11 and arbitrary one of the child chips 3, 7, 8 constituting the chip block 12. Furthermore, the interlevel wiring Lv can be provided to connect arbitrary ones of the wiring planes (first to third wiring planes 31 -33). It may connect non-adjacent ones of wiring planes, e.g. the first wiring plane 31 and the third wiring plane 33.

[0046]

The number of chip blocks 11, 12 may be one or three or more.

The child chip 6, at the above thereof, may be covered with polyimide resin 10. In this case, a heat-sink made of a metal foil (plate) or the like may be attached on a surface of the polyimide resin 10. Instead of polyimide resin 10, may be used a resin containing imide bond or acid bond or both imide and acid bonds. Alternatively, an insulator other than resin may be used.

[0047]

The parent chip 1, at its inactive surface, is not required to be connected with bumps 9. In this case, the semiconductor device can be mounted on a wiring board, for example, by applying cream solder to the electrode pad formed on the wiring board or the like and connecting it to the conductor 1d.

Figs. 2 to 5 are schematic sectional views for explaining a method for manufacturing a semiconductor device shown in Fig. 1. The semiconductor wafer 15 shown in Figs. 2 to 5 is the one in which, on a surface of the semiconductor wafer 15, a multiplicity of the regions corresponding to the parent chip 1 of semiconductor device in the final form shown in Fig. 1 are densely arranged. Although Fig. 2 to 5 each show only a region (unit region) corresponding to substantially one semiconductor device, the following

processes can be carried out commonly on every unit region.

[0048]

First, recesses 21 are formed in an active surface 15a of a semiconductor wafer 15 formed with internal-connection electrodes 1b, and then the conductor 1d is filled in the recesses 21. The semiconductor wafer 15, at this time, is greater in thickness than the parent chip 1 of the semiconductor device in the final form shown in Fig. 1. The semiconductor wafer 15 can have a thickness such that it has enough mechanical strength not to be broken during the semiconductor device manufacturing process. The thickness may be greater when using a greater diameter of semiconductor wafer 15. The recess 21 can be formed by drilling or laser working, for example. The conductor 1d can be filled in the recess 21 by using a conductor paste, for example.

[0049]

Similarly, recesses 22, 23 are respectively formed in the active surfaces 2a, 3a of the child chips 2, 3 formed with internal-connection electrodes 2b, 3b, and then conductors 2d, 3d are filled in the recesses 22, 23 (Fig. 2(a)). The child chip 2, 3, at this time, is greater in thickness than the child chip 2, 3 of the semiconductor device in the final form.

Then, the active surface 15a and the active surface 2a, 3a are placed opposed in parallel with each other (child chip

2, 3 put faced down), and the internal-connection electrode 2b, 3b is aligned with the corresponding internal-connection electrode 1b in a direction of the active surface 2a, 3a. Subsequently, the active surface 15a and the active surface 2a, 3a are put close to each other, to connect (join) the internal-connection electrode 1b and the internal-connection electrode 2b, 3b together. Thereafter, polyimide resin 10 is formed as covering the child chip 2, 3 on the active surface 15a (Fig. 2(b)). The polyimide resin 10 is formed as burying therein the inactive surface of the child chip 2, 3. The polyimide resin 10 can be obtained by applying, for example, a solution of polyamic acid, which is a precursor of polyimide resin 10, over the active surface 15a of the semiconductor wafer 15 and heating the precursor at a proper temperature.

[0050]

Then, polish (surface polish) is made on the surface of the polyimide resin 10. This process may be by physical abrasion or polish or by chemical polish (fusion) such as etching. When carrying out surface polish, for example, the semiconductor wafer 15 at its inactive surface can be held on a support plate through an adhesive tape or absorbed on a support plate capable of sucking it. By surface polish, the polyimide resin 10 is removed to expose the inactive surface of the child chip 2, 3. Furthermore, the polyimide

resin 10 and the inactive surface 2a, 3a of the child chip 2, 3 are polished to expose the conductor 2d, 3d in the recess 22, 23. Thereby, the recess 22, 23 turns into a penetration hole 2c, 3c penetrating the child chip 2, 3 in its thickness direction. This state is shown in Fig. 3(c).

[0051]

After surface polish, the inactive surface of the child chip 2, 3 and the surface of the polyimide resin 10 turn in to a first wiring plane 31 in flush. Even after exposing the conductor 2d, 3d, surface polish may be continued to obtain a desired thickness of child chip 2, 3, thus reducing the thickness of the child chip 2, 3. This makes it possible to reduce the thickness of the semiconductor device overall and the length of conductor 2d, 3d (wiring length) in a thickness direction of the child chip 2, 3.

[0052]

Because the child chip 2, 3 is mechanically protected by the polyimide resin 10, there is no possibility of damaging the child chip 2, 3 or the connection of the child chip 2, 3 with the semiconductor wafer 15 by the stress encountered during surface polish. Accordingly, the child chip 2, 3 can be made small in thickness.

Subsequently, on the first wiring plane 31, electrode pads 2e, 3e are respectively formed on the conductor 2d, 3d, and an intralevel wiring Lh1 is formed in a predetermined

position on an inactive surface of the child chip 3 and on a surface of polyimide resin 10 (Fig. 3(d)). Showing one example of forming electrode pads 2e, 3e and intralevel wiring Lh1, a predetermined surface area of the polyimide resin 10 is first treated by a solution of potassium hydroxide, to thereby open the polyimide ring in a surface of the polyimide resin 10 and introduce carboxyl group to the surface of the polyimide resin 10. By treating a surface of the polyimide resin 10 thus surface-reformed in a predetermined area by using a solution containing metal ions (e.g. copper sulfate solution), ion-exchange reaction is caused to form a thin metal film. After forming a thin metal film also in a predetermined position on the child chip 2, 3 by a proper process, electrolytic plating is carried out on these thin metal films by energizing them to increase the thickness thereof. Thus, it is possible to form films of electrode pads 2e, 3e and intralevel wiring Lh1. This can form electrode pads 2e, 3e and an intralevel wiring Lh1 in batch at the same time.

[0053]

Next, a recess 24, 27 is formed in an active surface 4a, 7a of the child chip 4, 7 formed with the internal-connection electrode 4b, 7b, to fill a conductor 4d, 7d in the recess 24, 27. The child chip 4, 7 at this time is greater in thickness than the chid chip 4, 7 of the

semiconductor device in the final form shown in Fig. 1. Then, the first wiring plane 31 and the active surfaces 4a, 7a are opposed in parallel with each other, to align the internal-connection electrodes 4b, 7b with the corresponding electrode pads 2e, 3e or the intralevel wiring Lh1 in a direction of the active surface 4a, 7a.

[0054]

Subsequently, the first wiring plane 31 and the active surfaces 4a, 7a are placed close to each other, to connect (join) the internal-connection electrode 4b, 7b and the electrode pad 2e, 3e, and the intralevel wiring Lh1 and the corresponding internal-connection electrodes. This connects the child chips 4, 7 face down on the first wiring plane 31. Thereafter, on the first wiring plane 31, polyimide resin 10 is formed as covering the child chips 4, 7 (Fig. 4(e)).

Surface polish is similarly carried out until the conductor 4d, 7d are exposed. This makes the recesses 24, 27 into penetration holes 4c, 7c. The inactive surface of child chip 4, 7 and the surface of polyimide resin 10 are made into a second wiring plane 32 in flush. Subsequently, on the second wiring plane 32, electrode pads 4e, 7e are formed on the conductor 4d, 7d and an intralevel wiring Lh2 is formed in a predetermined area on the inactive surface of the child chip 7 and on the surface of the polyimide resin 10.

[0055]

Furthermore, a similar process is carried out by using the child chips 5, 8 respectively formed with the internal-connection electrodes 5b, 8b. This connects the internal-connection electrodes 5b, 8b and electrode pads 4e, 7e and the intralevel wiring Lh2. The child chips 5, 8 is thickness-reduced by polish to form penetration holes 5c, 8c filled with conductor 5d, 8d. The inactive surface of the child chip 5, 8 and the surface of the polyimide resin 10 are made into a third wiring plane 33 in flush.

[0056]

In this state, a hole-opening process is carried out on the polyimide resin 10 at above a predetermined point of the intralevel wiring Lh2. This process can be made by laser working or etching. This forms a via hole 35 in a sectionally V-form in the polyimide resin 10 between the second wiring plane 32 and the third wiring plane 33, thereby exposing a part of the intralevel wiring Lh2 (Fig. 4(f)).

Thereafter, an electrode pad 5e, intralevel wirings Lh31, Lh32 and an interlevel wiring Lv are formed in predetermined positions. The interlevel wiring Lv is formed on an inner periphery of the via hole 35 and on an exposed portion of the intralevel wiring Lh2 from the bottom of the via hole 35. This process can be carried out by the method exemplified as the method for forming an intralevel wiring Lh1. This can integrate the intralevel wiring Lh31 and the

interlevel wiring Lv together, and these can be simultaneously formed with the electrode pad 5e and the intralevel wiring Lh32 in batch.

[0057]

Subsequently, a child chip 6 formed with an internal-connection electrode 6b on its active surface 6a is connected face down such that the internal-connection electrode 6b is joined to an electrode pad 5e and the intralevel wiring Lh31 (Fig. 5(g)). No recesses are formed in the child chip 6. After forming the polyimide resin 10 as covering the child chip 6 on the third wiring plane 33, surface polish is conducted until the child chip 6 has a predetermined thickness.

Furthermore, polish is made on the inactive surface of the semiconductor wafer 15 (backside polish) until the conductor 1d is exposed. This makes the recess 21 into a penetration hole 1c. After exposing the conductor 1d, backside polish may be continued in order to reduce the thickness of the semiconductor wafer 15. This can reduce the thickness of the entire semiconductor device and shorten the length (wiring length) of the conductor 1d in a thickness direction of the semiconductor wafer 15 (parent chip 1).

[0058]

During backside polish, the semiconductor wafer 15 will not be broken by backside polish because it is reinforced

by the polyimide resin 10 and the child chips 2 - 8 formed on the active surface 15a thereof. A bump 9, such as a solder ball, is connected to the exposed conductor 1d.

Thereafter, as shown in Fig. 5(h), the semiconductor wafer 15 is cut, together with the polyimide resin 10, along scribe lines S (cutting lines) by a dicing saw 29. Thereby, from the semiconductor wafer 15 is cut an individual piece of semiconductor device having a parent chip 1 joined thereon with child chips 2 - 8 as shown in Fig. 1.

[0059]

The above manufacturing method is an example that each process is carried out, in batch, on the regions corresponding to a plurality of semiconductor devices on the semiconductor wafer 15. With the manufacturing method like this, a plurality of chip-on-chip-structured semiconductor devices can be manufactured with efficiency. However, the invention is not limited to this, and the process may be carried out on one piece of parent chip 1 to obtain such a semiconductor device.

The via hole 35 for forming an interlevel wiring Lv may be formed by drilling. In this case, obtained is a via hole 35 having a nearly constant diameter with respect to the thickness direction of the polyimide resin 10, which, however, has no effect upon forming an interlevel wiring Lv by using ion exchange or the like. In a case where there is no need

to form intralevel wiring Lh1, Lh2, Lh31, Lh32 in batch with an interlevel wiring Lv, unwanted portions may be removed by etching after laminating metal foils (e.g. copper foils) over the entire surfaces of the first to third wiring planes 31 - 33.

[0060]

Other various modifications can be made within the scope of the description in the scope of claims.

[Brief Description of Drawings]

[Fig. 1]

A schematic sectional view showing a structure of a semiconductor device according to an embodiment of the present invention.

[Fig. 2]

A schematic sectional view for explaining first processes in a method for manufacturing a semiconductor device according to an embodiment of the present invention.

[Fig. 3]

A schematic sectional view for explaining processes following the processes shown in Fig. 2.

[Fig. 4]

A schematic sectional view for explaining processes following the processes shown in Fig. 3.

[Fig. 5]

A schematic sectional view for explaining processes

following the processes shown in Fig. 4.

[Explanation of Reference Numerals]

1 parent chip

2 - 8 child chip

1a - 8a, 15a active surface

1b - 8b internal-connection electrode

1c - 5c, 7c, 8c penetration hole

1d - 5d, 7d, 8d conductor

Lh1, Lh2, Lh31, Lh32 intralevel wiring

Lv interlevel wiring

10 polyimide resin

11 first chip block

12 second chip block

15 semiconductor wafer

21 - 25, 27, 28 recess

31 first wiring plane

32 second wiring plane

33 third wiring plane

[Document Name] Drawings

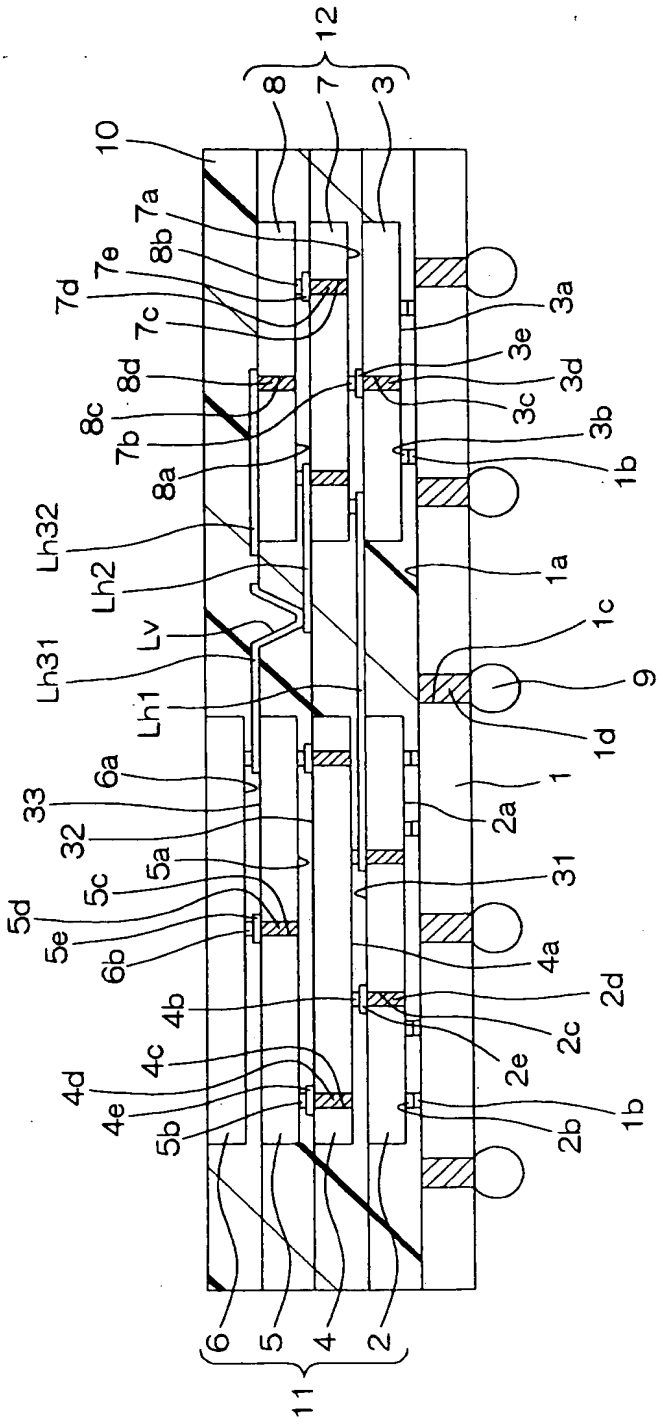


FIG. 1

FIG. 2

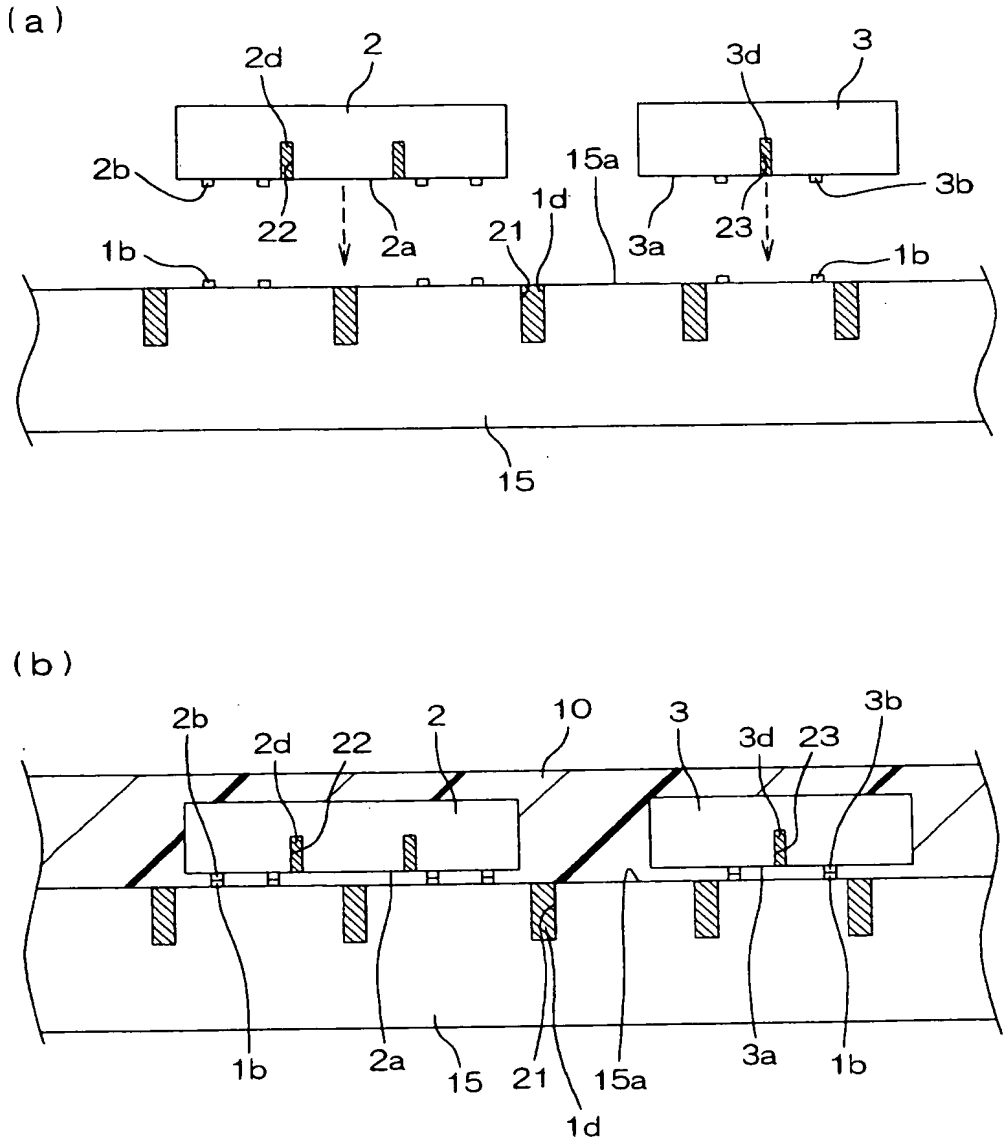
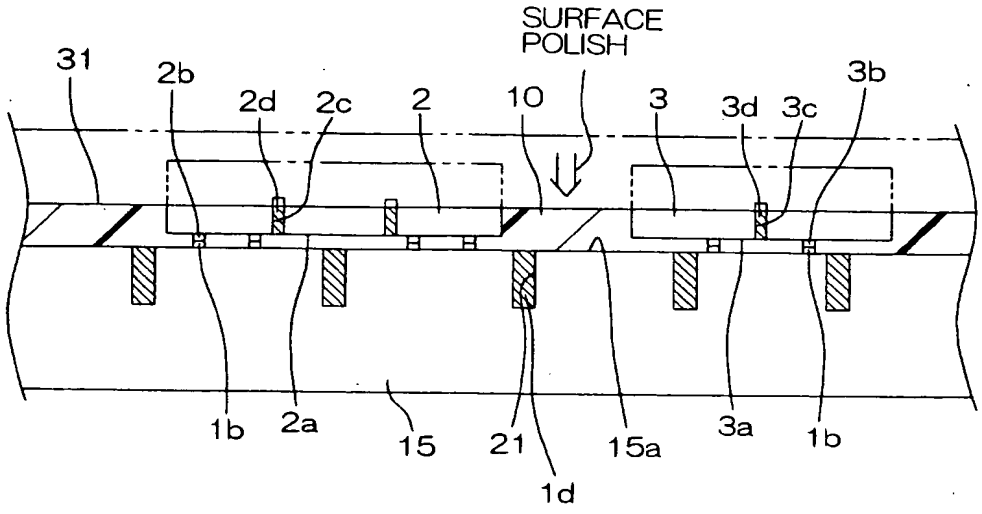

(a)
2d
2
3d
3
2b
15a
3b
1d
22
2a
21
3a
23
1b
1b
15
(b)
2b
2d
22
2
10
3
3d
23
3b
1b
2a
15
21
15a
3a
1b
1d

FIG. 3

(c)


SURFACE
POLISH
31
2b
2d
2c
2
10
3
3d
3c
3b
1b
2a
15
21
15a
3a
1b
1d

(d)

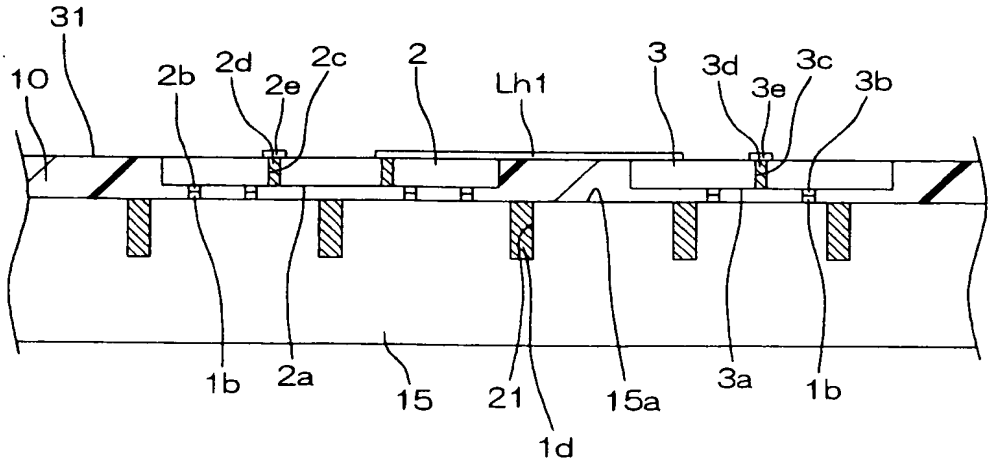
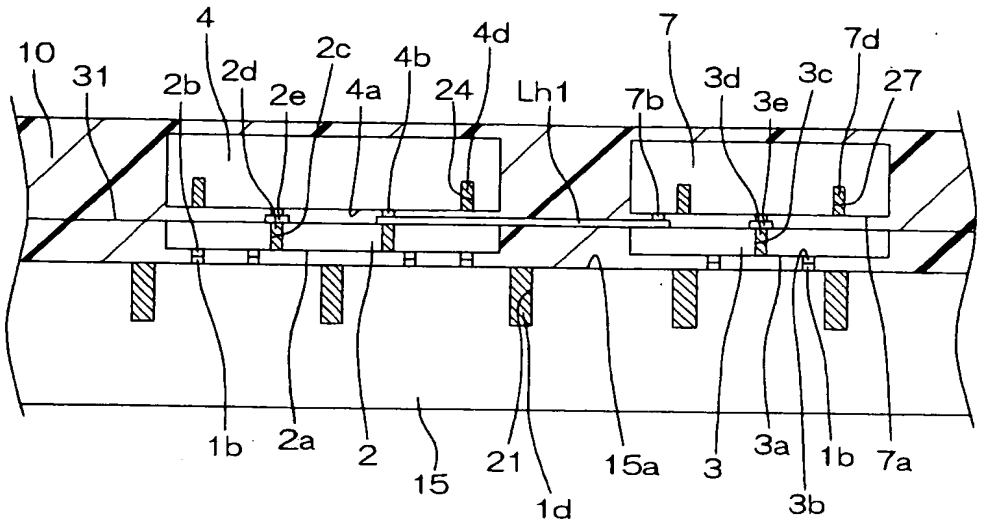
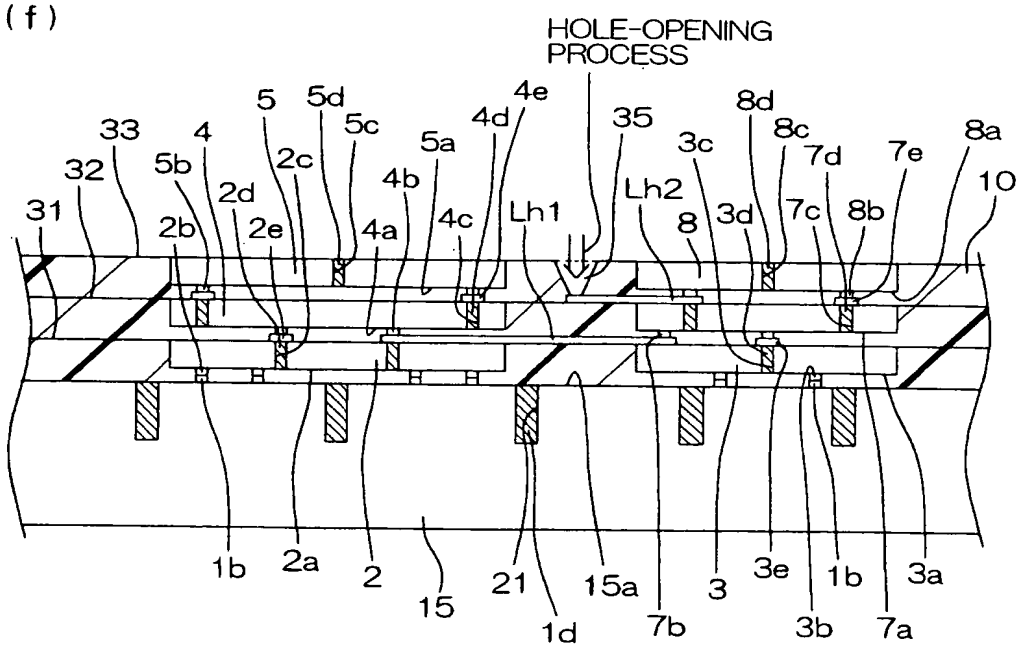

31
10
2b
2d
2e
2c
2
Lh1
3
3d
3e
3c
3b
1b
2a
15
21
15a
3a
1b
1d

FIG. 4

(e)


10
31
4
2b
2d
2e
2c
4a
4b
24
4d
Lh1
7
7b
3d
3e
3c
7d
27
1b
2a
2
15
21
1d
15a
3
3a
1b
3b
7a

(f)


HOLE-OPENING PROCESS
33
32
31
4
5b
2b
5
5d
2d
2c
2e
5c
4a
5a
4b
4c
4d
4e
Lh1
35
Lh2
8
3c
3d
8d
8c
7d
7c
7e
8b
8a
10
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15
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1d
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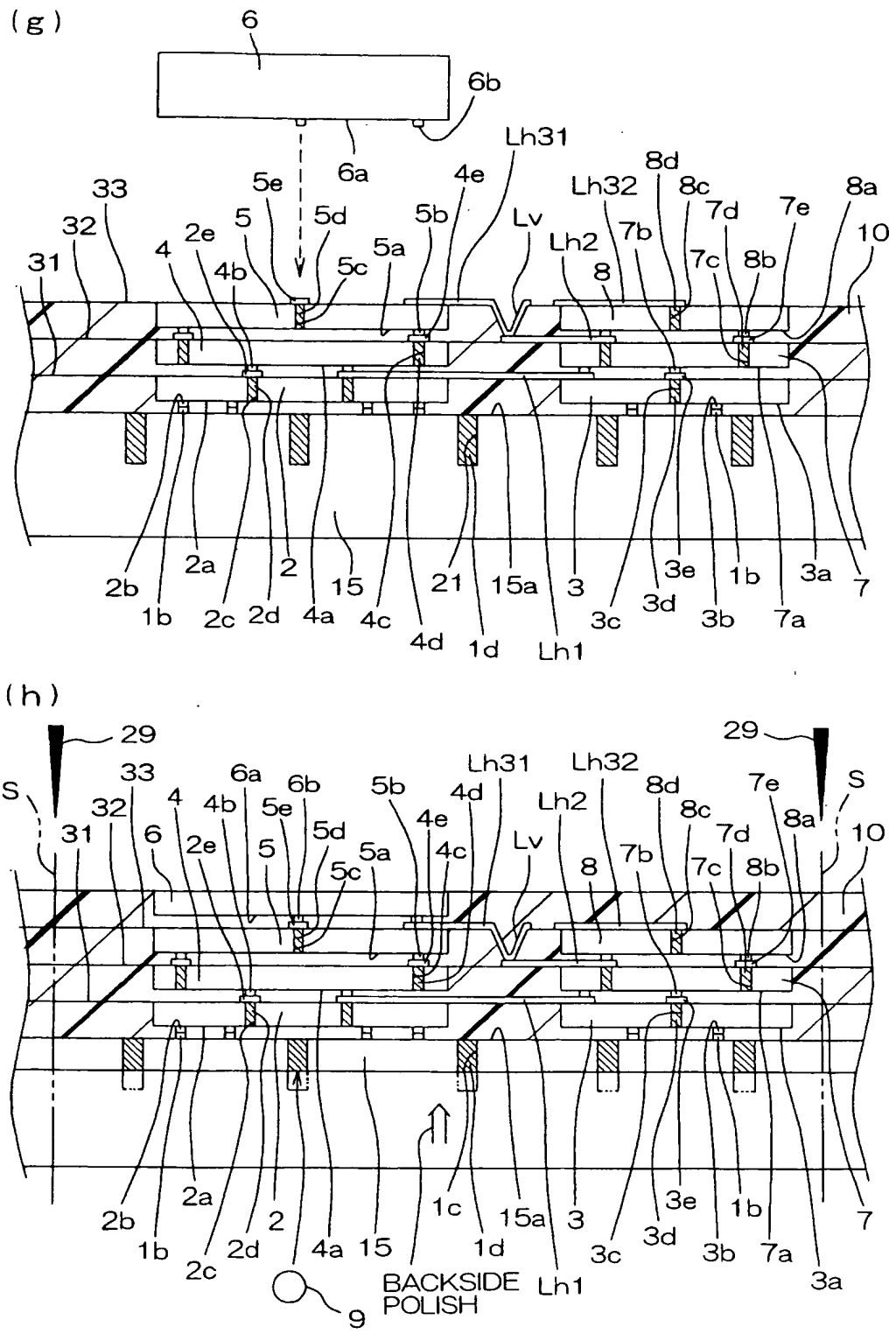
7b
3
3e
3b
1b
7a
3a

FIG. 5


(g)
6
6b
6a
Lh31
33
5e
4e
8d
32
5
5d
5b
Lv
Lh32
8c
7d
7e
8a
2e
7b
Lh2
10
31
4
4b
5c
5a
8
7c
8b
2b
2a
2
15
21
15a
3
3e
1b
3a
7
1b
2c
2d
4a
4c
4d
1d
Lh1
3c
3d
3b
7a
(h)
29
29
S
S
33
6a
6b
5b
Lh31
Lh32
32
4
4b
5e
4d
Lh2
8d
7e
31
6
2e
5
5d
4e
8c
8a
10
5a
4c
Lv
7d
8
7b
7c
8b
2b
2a
1c
15a
3
3e
1b
7
1b
2c
2d
2
4a
15
1d
3c
3d
3b
7a
3a
9
BACKSIDE POLISH
Lh1

[Document Name] Abstract

[Abstract]

[Problem]

To provide a semiconductor device increased in integration degree and low in manufacture cost and a manufacturing method of the same.

[Solution to the Problem]

Child chips 2, 4 - 6 and child chips 3, 7, 8 are sequentially superposed on an active surface 1a of a parent chip 1. Penetration holes 2c - 5c, 7c, 8c penetrating the child chips 2 - 5, 7, 8 in the thickness direction are formed on the child chips 2 - 5, 7, 8. Conductors 2d - 5d, 7d, 8d are filled in the penetration holes 2c - 5c, 7c, 8c. Internal-connection electrodes 2b - 8b are formed in inactive surfaces 2a - 8a of the child chips 2 - 8. The internal-connection electrodes 4b - 8b are joined to the conductors 2d, 4d, 5d, 3d, 7d via electrode pads 2e, 4e, 5e, 3e, 7e, whereby the child chips 4 - 8 are electrically connected to the child chips 2, 4, 5, 3, 7 adjacent below.

[Representative Drawing] Fig. 1